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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/324,823	06/02/1999	TAKESHI IDE	P99.0654	2056

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EXAMINER
MOE, AUNG SOE

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 03/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/324,823	Applicant(s) Takeshi Ide et al.
	Examiner Aung Moe	Art Unit 2612

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 17, 2002*

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideratio

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-3* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examine

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuba (U.S. 5,523,787) in view of Suzuki (U.S. 5,828,407).

Regarding claim 1, Fukuba '787 discloses a solid-state image sensor (Figs. 1 and 4) device having an image sensing portion performing photoelectric conversion in unit of picture elements and being able to correspond to both progressive mode in which all picture element

signals obtained by the scanning of one time in said image sensing portion being output independently (i.e., noted the Full Frame transfer mode as discussed in col. 1, lines 20+), and interlace mode in which a plurality of times of interlaced scanning being performed and the picture element signals obtained in respective scannings in said image sensing portion being superposed (i.e., noted the interlaced mode for displaying moving images as discussed in col. 1, lines 30-35).

Furthermore, it is noted that although Fukuba '787 discloses the CCD device capable of operating at both the progressive mode (i.e., Full frame mode for capturing a still image as discussed in col. 1, lines 20+) and the interlace mode (i.e., the moving/monitor mode for capturing and displaying a moving image as discussed in col. 1,lines 30+), Fukuba '787 does not explicitly show the use of a substrate-bias generation circuit for applying a basis voltage to the substrate of said image sensing portion and for controlling said bias voltage in said progressive mode to be smaller than said voltage in said interlaced mode as recited in present claimed invention.

However, the above mentioned claimed limitations are well-known in the art as evidenced by Suzuki '407. In particular, Suzuki '407 discloses that it is conventionally well-known in the art to use a substrate-bias generation circuit for applying a basis voltage (i.e., Fig. 1, the elements' 2, 3 and 4) to the substrate of said image sensing portion (i.e., the CCD sensor of the camera as shown in Fig. 1 of Suzuki '407) and for controlling said bias voltage in said progressive mode (i.e., the Finder/motion mode as discussed in col. 7, lines 25+ of Suzuki '407)

to be smaller than said voltage in said interlaced mode (i.e., noted from the Fig. 14 of Suzuki '407 that the Vsub2 for the Frame Mode for producing the still image is less than the Vsub1 of the Filed mode for producing the interlaced moving image for displaying the moving image therein; see Fig. 14 and col. 3, lines 45+, col. 7, line 20 -col. 8, lines 45) as recited in present claimed invention.

In view of the above, having the system of Fukuba '787 and then given the well-established teaching of Suzuki '407, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Fukuba '787 as taught by Suzuki '407, since Suzuki '407 states at col. 3, lines 55+ and col. 4, lines 50+ that such a modification would increase the capacitance of a pixel thereby improving dynamic range when the still image is sensed in the frame mode.

Regarding claim 2, Fukuba '787 discloses a drive method for a solid-state image sensor device (i.e., Figs. 1 and 4) having an image sensing portion performing photoelectric conversion in the unit of picture elements and being able to correspond to both progressive mode in which all picture element signals obtained by scanning of one time in said image sensing portion are output independently (i.e., noted the Full Frame transfer mode as discussed in col. 1, lines 20+), and interlaced mode in which a plurality of times of interlaced scanning being performed and picture element signals obtained in respective scannings being superposed (i.e., noted the interlaced mode for displaying the moving image as discussed in col. 1, lines 30-35).

Furthermore, it is ntoed that although Fukuba '787 discloses the CCD device capable of operating at both the progressive mode (i.e., Full frame mode for capturing a still image as discussed in col. 1, lines 20+) and the interlace mode (i.e., the moving/monitor mode for capturing and displaying a moving image as discussed in col. 1,lines 30+), Fukuba '787 does not explicitly show wherein in applying a bias voltage to the substrate of said image sensing portion, in said progressive mode the value of said bias voltage being made smaller than that in said interlace mode as recited in present claimed invention.

However, the above mentioned claimed limitations are well-known in the art as evidenced by Suzuki '407. In particular, Suzuki '407 discloses that it is conventionally well-known in the art to use a substrate-bias generation circuit for applying a basis voltage (i.e., Fig. 1, the elements' 2, 3 and 4) to the substrate of said image sensing portion (i.e., the CCD sensor of the camera as shown in Fig. 1 of Suzuki '407) and for controlling the applying process of the bias voltage in said progressive mode (i.e., the Finder/motion mode as discussed in col. 7, lines 25+ of Suzuki '407) and the interlaced mode (i.e., the Finder mode as discussed in col. 25+ of Suzuki '407), and

wherein in applying a bias voltage to the substrate of said image sensing portion, in said progressive mode the value of said bias voltage being made smaller than that in said interlace mode (i.e., noted from the Fig. 14 of Suzuki '407 that the Vsub2 for the Frame Mode for producing the still image is less than the Vsub1 of the Filed mode for producing the interlaced

moving image for displaying the moving image therein; see Fig. 14 and col. 3, lines 45+, col. 7, line 20 -col. 8, lines 45) as recited in present claimed invention.

In view of the above, having the system of Fukuba '787 and then given the well-established teaching of Suzuki '407, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Fukuba '787 as taught by Suzuki '407, since Suzuki '407 states at col. 3, lines 55+ and col. 4, lines 50+ that such a modification would increase the capacitance of a pixel thereby improving dynamic range when the still image is sensed in the frame mode.

Regarding claim 3, Fukuba '787 discloses a camera being composed of a solid-state image sensor device having an image sensing portion performing photoelectric conversion in unit of picture elements (i.e., noted from col. 1, lines 15+ of Fukuba '787 that the CCD sensor is used in the imaging device such as a camera) and a substrate-bias generation circuit, an optical system leading in an incident light from a subject and forming an image on said image sensing portion of said solid-state image sensor device, and a signal processing system for processing the signals output from said solid-state image sensor device to obtain a video signal (i.e., noted that a substrate-bias generating circuit, an optical system and the signals processing system are considered as the inherent features of the conventional camera, thus, such features have to be included in the conventional camera system of Fukuba '787),

wherein said driving system for driving said solid state image sensor device in changing over selectively (i.e., noted that the imaging system of Fukuba '787 is capable of operating in

both Full frame mode for producing a still image and the interlace mode for displaying the moving image therein, thus, the selection of such modes as considered inherent) between progressive mode (i.e., noted the Full Frame transfer mode as discussed in col. 1, lines 20+) in which all picture element signals obtained by the scanning of one time in said image sensing portion being output independently, and interlaced mode in which the scannings of a plurality times being performed and the picture element signals obtained in respective scannings in said image sensing portion being superposed (i.e., noted the interlaced mode for displaying the moving image as discussed in col. 1, lines 30-35).

Furthermore, it is noted that although Fukuba '787 discloses the CCD device capable of operating at both the progressive mode (i.e., Full frame mode for capturing a still image as discussed in col. 1, lines 20+) and the interlace mode (i.e., the moving/monitor mode for capturing and displaying a moving image as discussed in col. 1,lines 30+), Fukuba '787 does not explicitly show that the bias voltage to be applied to the substrate in said progressive mode being controlled to be smaller than that in said interlaced mode by said substrate-bias generation circuit as recited in the present claimed invention.

However, the above mentioned claimed limitations are well-known in the art as evidenced by Suzuki '407. In particular, Suzuki '407 discloses that it is conventionally well-known in the art to use a substrate-bias generation circuit for applying a basis voltage (i.e., Fig. 1, the elements' 2, 3 and 4) to the substrate of said image sensing portion (i.e., the CCD sensor of the camera as shown in Fig. 1 of Suzuki '407) and for controlling said bias voltage in said

progressive mode (i.e., the Finder/motion mode as discussed in col. 7, lines 25+ of Suzuki '407) to be smaller than said voltage in said interlaced mode (i.e., noted from the Fig. 14 of Suzuki '407 that the Vsub2 for the Frame Mode for producing the still image is less than the Vsub1 of the Filed mode for producing the interlaced image data for displaying the moving image therein; see Fig. 14 and col. 3, lines 45+, col. 7, line 20 -col. 8, lines 45) as recited in present claimed invention.

In view of the above, having the system of Fukuba '787 and then given the well-established teaching of Suzuki '407, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Fukuba '787 as taught by Suzuki '407, since Suzuki '407 states at col. 3, lines 55+ and col. 4, lines 50+ that such a modification would increase the capacitance of a pixel thereby improving dynamic range when the still image is sensed in the frame mode.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Oda '291, Ueno '276 and Suzuki '703 shows a solid-state image sensor haivng a driving circuit, an optical system, a substrate-bias voltage generation circuit and the processing system thereof.

b. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Aung S. Moe** whose telephone number is **(703) 306-3021.** If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Wendy Garber**, can be reach on (703) 305-4929.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to the customer service number **(703) 306-0377.**

AUNG S. MOE
PATENT EXAMINER

A. Moe

March 7, 2003